

EXPRESS MAIL LABEL NO.: EL563155563US

WHAT IS CLAIMED IS:

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1. An arithmetic circuit for use with an RNS, said arithmetic circuit comprising:
an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs;
test circuitry coupled to the arithmetic core, the test circuitry inducing oscillation at the output of the arithmetic core during testing; and
logic circuitry coupled to the output of the arithmetic core, the logic circuitry producing a pass/fail signal based on whether the oscillation frequency of the arithmetic core is at least equal to a minimum threshold value.
 2. The arithmetic circuit as defined in claim 1, wherein the logic circuitry includes:
a counter coupled to the output of the arithmetic core, the counter counting oscillations of the output during testing; and
a comparator coupled to the counter, the comparator comparing the output of the counter after a predetermined test period with the minimum threshold value and producing the pass/fail signal.
 3. The arithmetic circuit as defined in claim 2, wherein the test circuitry includes:
a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and
at least one transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core during testing.
 4. The arithmetic circuit as defined in claim 3, wherein the isolation buffers, the transmission gate, and the counter are controlled by a test enable signal.

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5. The arithmetic circuit as defined in claim 1, wherein the test circuitry includes:
a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and
at least one transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core during testing.
6. The arithmetic circuit as defined in claim 1, wherein the test circuitry includes:
a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing;
a first transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core during testing; and
a second transmission gate for supplying a constant to the other input of the arithmetic core during testing.
7. The arithmetic circuit as defined in claim 6, wherein the isolation buffers and the transmission gates are controlled by a test enable signal.
8. The arithmetic circuit as defined in claim 1, wherein the arithmetic core is an OHRNS modulo m adder.
9. The arithmetic circuit as defined in claim 1, wherein the arithmetic core is an OHRNS modulo m multiplier.

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10. A digital signal processing device having at least one RNS arithmetic circuit, said arithmetic circuit comprising:

an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs;

test circuitry coupled to the arithmetic core, the test circuitry inducing oscillation at the output of the arithmetic core during testing; and

logic circuitry coupled to the output of the arithmetic core, the logic circuitry producing a pass/fail signal based on whether the oscillation frequency of the arithmetic core is at least equal to a minimum threshold value.

11. The digital signal processing device as defined in claim 10, wherein the logic circuitry of the arithmetic circuit includes:

a counter coupled to the output of the arithmetic core, the counter counting oscillations of the output during testing; and

a comparator coupled to the counter, the comparator comparing the output of the counter after a predetermined test period with the minimum threshold value and producing the pass/fail signal.

12. The digital signal processing device as defined in claim 11, wherein the test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and

at least one transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core during testing.

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13. The digital signal processing device as defined in claim 10, wherein the test circuitry of the arithmetic circuit includes:
 - a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing; and
 - at least one transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core during testing.
14. The digital signal processing device as defined in claim 10, wherein the test circuitry of the arithmetic circuit includes:
 - a plurality of isolation buffers for isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing;
 - a first transmission gate for feeding the output of the arithmetic core back to one of the inputs of the arithmetic core during testing; and
 - a second transmission gate for supplying a constant to the other input of the arithmetic core during testing.
15. The digital signal processing device as defined in claim 14, wherein the isolation buffers and the transmission gates are controlled by a test enable signal.
16. The digital signal processing device as defined in claim 10, wherein the arithmetic core of the arithmetic circuit is an OHRNS modulo m adder.
17. The digital signal processing device as defined in claim 10, wherein the arithmetic core of the arithmetic circuit is an OHRNS modulo m multiplier.

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18. A method for testing propagation delay of an RNS arithmetic circuit incorporated into an integrated circuit device, the arithmetic circuit including an arithmetic core that performs an RNS arithmetic operation, said method comprising the steps of:
- feeding the output of the arithmetic core back to one of the inputs of the arithmetic core;
- providing a constant to another input of the arithmetic core so as to induce oscillation at the output of the arithmetic core; and
- producing a pass/fail signal based on whether the oscillation frequency of the arithmetic core is at least equal to a minimum threshold value.
19. The method as defined in claim 18, wherein the step of producing a pass/fail signal includes the sub-steps of:
- counting oscillations of the output of the arithmetic core during a predetermined time period; and
- comparing the counted oscillations with the minimum threshold value to determine a pass or fail condition.
20. The method as defined in claim 19, further comprising the step of isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing.
21. The method as defined in claim 18, further comprising the step of isolating the inputs and output of the arithmetic core from upstream and downstream circuitry during testing.
22. The method as defined in claim 21, further comprising the step of supplying a test enable signal to start testing.

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23. The method as defined in claim 18, wherein the arithmetic core is an OHRNS modulo m adder.
 24. The method as defined in claim 18, wherein the arithmetic core of the arithmetic circuit is an OHRNS modulo m multiplier.